WHAT IS CLAIMED IS:

1. A method for forming a tri-gate semiconductor device that includes a substrate and a dielectric layer formed on the substrate, comprising:

depositing a first dielectric layer on the dielectric layer;

etching the first dielectric layer to form a structure;

depositing a second dielectric layer over the structure;

depositing an amorphous silicon layer over the second dielectric layer;

etching the amorphous silicon layer to form amorphous silicon spacers, the amorphous silicon spacers being disposed on opposite sides of the structure;

depositing a metal layer on at least an upper surface of each of the amorphous silicon spacers;

annealing the metal layer to convert the amorphous silicon spacers to crystalline silicon fin structures;

removing a portion of the second dielectric layer;

depositing a gate material; and

etching the gate material to form three gates.

2. The method of claim 1 wherein the depositing a first dielectric layer includes:

depositing the first dielectric layer to a thickness ranging from about 600 Å to about 1000 Å.

3. The method of claim 1 wherein the first dielectric layer comprises silicon dioxide.

4. The method of claim 1 wherein a width of the structure ranges from about 500 Å to about 2000 Å.

5. The method of claim 1 wherein the depositing a second dielectric layer includes:

depositing the second dielectric layer to a thickness ranging from about 200 Å to about 300 Å.

6. The method of claim 5 wherein the first and second dielectric layers comprise silicon dioxide.

7. The method of claim 1 wherein the depositing an amorphous silicon layer includes:

depositing the amorphous silicon layer to a thickness ranging from about 150 Å to about 300 Å.

8. The method of claim 1 wherein a width of each of the amorphous silicon spacers ranges from about 50 Å to about 200 Å.

9. The method of claim 1 wherein the depositing a metal layer includes:

depositing a nickel layer to a thickness ranging from about 20 Å to about 30 Å.

10. The method of claim 1 wherein the annealing includes:

annealing the metal layer at a temperature of about 500 °C to about 550 °C.

11. The method of claim 1 wherein the depositing a gate material includes:

depositing a polysilicon layer to a thickness ranging from about 200 Å to about 1000 Å.

12. A method of manufacturing a semiconductor device that includes a substrate and a nitride layer formed on the substrate, the method comprising:

depositing a first silicon oxide layer on the nitride layer;

etching the first silicon oxide layer to form a structure, the structure having at least a first side surface, a second side surface, and a top surface;

depositing a second silicon oxide layer over the top surface and surrounding the first and second side surfaces of the structure;

depositing an amorphous silicon layer over the second silicon oxide layer;

etching the amorphous silicon layer to form amorphous silicon structures, a first amorphous silicon structure being formed on a first side of the structure and a second amorphous silicon structure being formed on a second side of the structure;

depositing a metal layer on at least an upper surface of each of the amorphous silicon structures;

performing a metal-induced crystallization operation to convert the amorphous silicon structures to crystalline silicon structures;

removing a portion of the second silicon oxide layer;

forming a source region and a drain region;

depositing a gate material over at least the crystalline silicon structures; and

patterning and etching the gate material to form three gate electrodes.

13. The method of claim 12 wherein the depositing a second silicon dioxide layer includes:

depositing the second silicon dioxide layer to a thickness ranging from about 200 Å to about 300 Å.

14. The method of claim 12 wherein the depositing an amorphous silicon layer includes:

depositing the amorphous silicon layer to a thickness ranging from about 150 Å to about 300 Å.

15. The method of claim 14 wherein a width of each of the amorphous silicon spacers ranges from about 50 Å to about 200 Å.

16. The method of claim 12 wherein the performing a metal-induced crystallization operation includes:

annealing the metal layer at a temperature of about 500 °C to about 550 °C.

17. A semiconductor device comprising:

a structure comprising a dielectric material and including a first side and a second side;

a first fin structure comprising a crystalline silicon material and being formed adjacent to the first side of the structure;

a second fin structure comprising the crystalline silicon material and being formed adjacent to the second side of the structure;

a source region formed at one end of the structure, the first fin structure, and the second fin structure;

a drain region formed at an opposite end of the structure, the first fin structure, and the second fin structure;

a first gate formed adjacent the first fin structure;

a second gate formed adjacent the second fin structure; and

a third gate formed above the first fin structure and the second fin structure.

18. The semiconductor device of claim 17 further comprising:

a nitride layer, the structure being formed on the nitride layer.

19. The semiconductor device of claim 18 wherein the first fin structure and the second fin structure are formed at about 100 Å to about 500 Å above the nitride layer.

20. The semiconductor device of claim 17 wherein a width of the first fin structure and the second fin structure ranges from about 50 Å to about 200 Å.